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AN/TPQ-37 TRANSMITTER TEST BED.(U)
FEB 79 W L MCPEAK, E J BONEM DAAB07-78-C-3010

UNCLASSIFIED FR-79-14-261 DELET-TR-78-3010-1 NL

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Research and Development Technical Report
DELET-TR-78-3010-1

AD A069975

AN/TPQ-37 TRANSMITTER TEST BED

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FEB 1979

First Interim Report for Period October 1978 Through January 1979

Prepared for

ERADCOM

ELECTRONICS TECHNOLOGY AND DEVICES LABORATORY
US ARMY ELECTRONICS COMMAND FORT MONMOUTH, NEW JERSEY 07703

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REPORT DOCUMENTATION PAGE		READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER 18 DELET-TR-78-C-3001-1	2. GOVT ACCESSION NO.	3. RECIPIENT'S CATALOG NUMBER 9
4. TITLE (and Subtitle) 6 AN/TPQ-37 TRANSMITTER TEST BED.		5. TYPE OF REPORT & PERIOD COVERED [redacted] Interim rept. no. 1, Oct 78-[redacted] Jan 79,
		6. PERFORMING ORG. REPORT NUMBER 14 FR-79-14-261
7. AUTHOR(s) 10 W. L. McPeak, E.J. Bonem		8. CONTRACT OR GRANT NUMBER(s) 15 DAAB07-78C-3010
9. PERFORMING ORGANIZATION NAME AND ADDRESS Hughes Aircraft Company, Ground Systems Group, 1901 W. Malvern, Fullerton, CA 92634		10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS 16 IL2 63742 DF 32 01.B3
11. CONTROLLING OFFICE NAME AND ADDRESS W15P87 – US Army Electronics Research and Development Command, USAERADCOM, Attn: ET&D Lab, DELET-BM, Fort Monmouth, N.J. 07703		12. REPORT DATE 11 Feb [redacted] 79
		13. NUMBER OF PAGES 35 (17 Ø1)
14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office) 12 35p		15. SECURITY CLASS. (of this report) Unclassified
		15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT (of this Report)

Approved for Public Release

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

18. SUPPLEMENTARY NOTES

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Fault Isolation
Microprocessor
High Power
TWT Design
Microwave Transmitter

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The AN/TPQ-37 Transmitter Test Bed will provide a vehicle for evaluating techniques for improving the reliability and maintainability of the AN/TPQ-37 Transmitter. Work includes design and fabrication of a major portion of the microprocessor based fault isolation subsystem.

Support has been provided to ERADCOM in initiating procurement of Advanced Design Traveling Wave Tubes. During a later phase of the program these TWT's will be evaluated in the AN/TPQ-37 Transmitter.

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Section S

SUMMARY

The AN/TPQ-37 Transmitter Test Bed will provide a vehicle for evaluating techniques for improving the reliability and maintainability of the AN/TPQ-37 Transmitter. Work includes design and fabrication of a major portion of the microprocessor based fault isolation subsystem.

Support has been provided to ERADCOM in initiating procurement of Advanced Design Traveling Wave Tubes. During a later phase of the program these TWT's will be evaluated in the AN/TPQ-37 Transmitter.

Remaining tasks of the AN/TPQ-37 Test Bed Program have not yet been scheduled or initiated. These tasks will be started when availability of the transmitter to be used for the testing is identified by the government.

Progress during this reporting period on the AN/TPQ-37 Test Bed Program includes:

- Design of fault isolation subsystem components.
- Fabrication of breadboard circuits needed for testing and evaluating the detailed fault isolation subsystem.
- Circuits to implement the automatic cathode current control loop have been included in the fault isolation circuits.
- Closed loop TWT automatic RF drive level control techniques are being studied.
- Participated in meetings at Varian Associates and Hughes Electron Dynamics Division to review their progress on their Advanced Traveling Wave Tube design programs.

CONTENTS

SECTION 1
INTRODUCTION

Section 1

INTRODUCTION

1.1 PROGRAM OBJECTIVES

The AN/TPQ-37 Transmitter Test Bed will provide a vehicle for evaluating techniques for improving the reliability and maintainability of the AN/TPQ-37 transmitter.

The specific objectives of this program are:

1. To evaluate Advanced Design Traveling Tubes resulting from USAERADCOM solicitation DAAB07-78Q-2082.
2. To design, develop, and evaluate in a AN/TPQ-37 transmitter a microprocessor based fault isolation subsystem that will report malfunctions in a maintenance oriented manner.
3. To design, develop, and evaluate a closed loop automatic cathode current control loop.
4. To design, develop, and evaluate an automatic RF drive level control loop.
5. To evaluate in an AN/TPQ-37 transmitter the solid state floating deck grid modulator developed under contract DAAB07-77-C-2647.
6. To design, develop, and evaluate an improved inverter communtating choke.

1.2 PROGRAM ORGANIZATION

The objectives of this program will be accomplished in three major phases:

The first phase will include the independent development and testing of the new components and circuits, which include:

- Support procurement of an advanced design TWT.
- Design a new, cased transformer for use with the solid state grid modulator.
- Fault isolation circuits and control loop circuits.
- Improved commutating choke design.

The second phase will consist of installation of the new hardware into the AN/TPQ-37 Test Bed Transmitter and evaluation of transmitter performance.

The last phase will include development of recommendations accumulated during the test phase and presentation of the recommendations in the final report.

SECTION 2
PROGRESS

Section 2

PROGRESS

2.1 ADVANCED DESIGN TRAVELING WAVE TUBE

Program reviews have been conducted jointly with ERADCOM at both Varian Assoc. and Hughes Electron Dynamics Division to monitor their approaches to achieve TWT improvements. Both companies have ordered material and are in the process of assembling their first electron gun.

2.2 FAULT ISOLATION

During this first reporting period the circuits needed for detailed fault isolation were designed, fabricated and initial testing was begun. Photographs of the cards containing this circuitry are shown in Figures 1 through 3.

The fault isolation circuits are shown in the block diagram of Figure 4, and divide into three functional parts:

1. microprocessor based controller card
2. three types of monitor cards
3. display device

2.2.1 Controller Card

The Controller Card utilized a Intel 8080A microprocessor. The function of this card is primarily to tabulate status information provided by the monitor circuits. From this information, the microprocessor verifies the operation of each line replaceable unit (LRU). Finally the processor reports any malfunction and the source of the malfunction to the display device.

2.2.2 Monitor Cards

These cards provide the interface to the transmitter units, and provide transmitter status information to the controller card. This circuitry is contained on several cards including:

1. Inverter Monitor: Monitors the operation of the TWT beam power supply inverter and rectifier assembly.

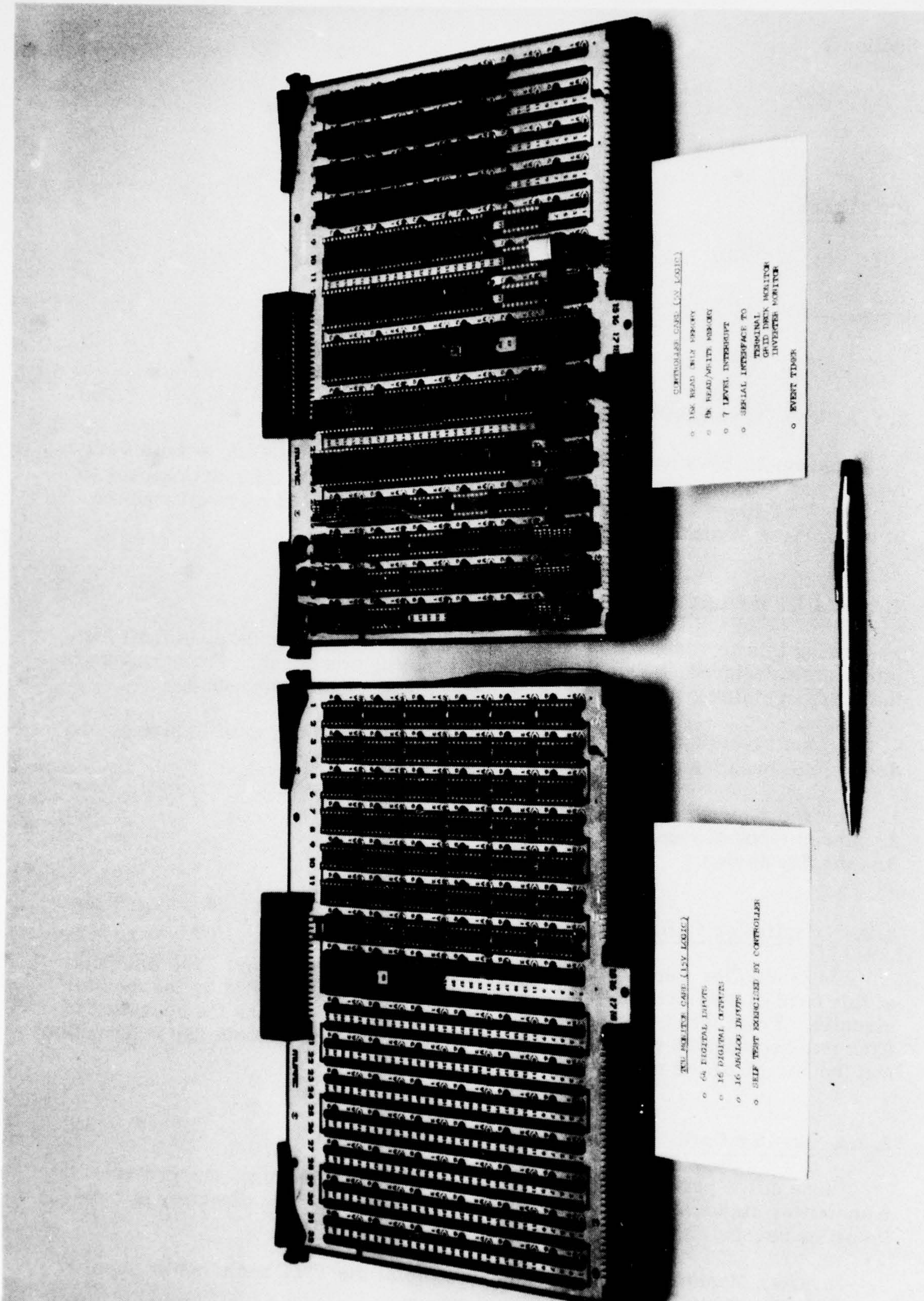

FIGURE 1 CONTROLLER CARD AND TCU MONITOR CARD

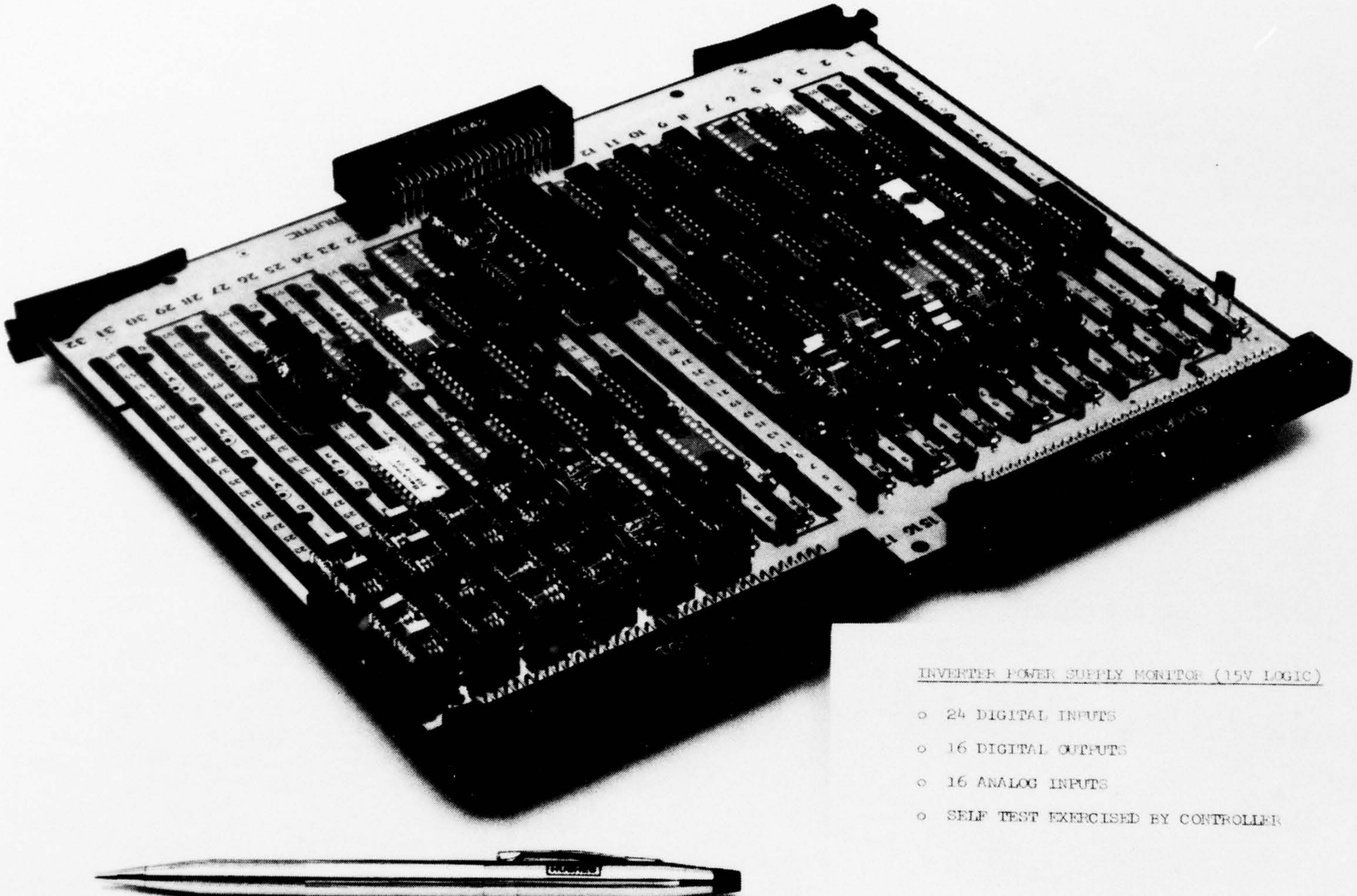

FIGURE 2 INVERTER POWER SUPPLY MONITOR CARD

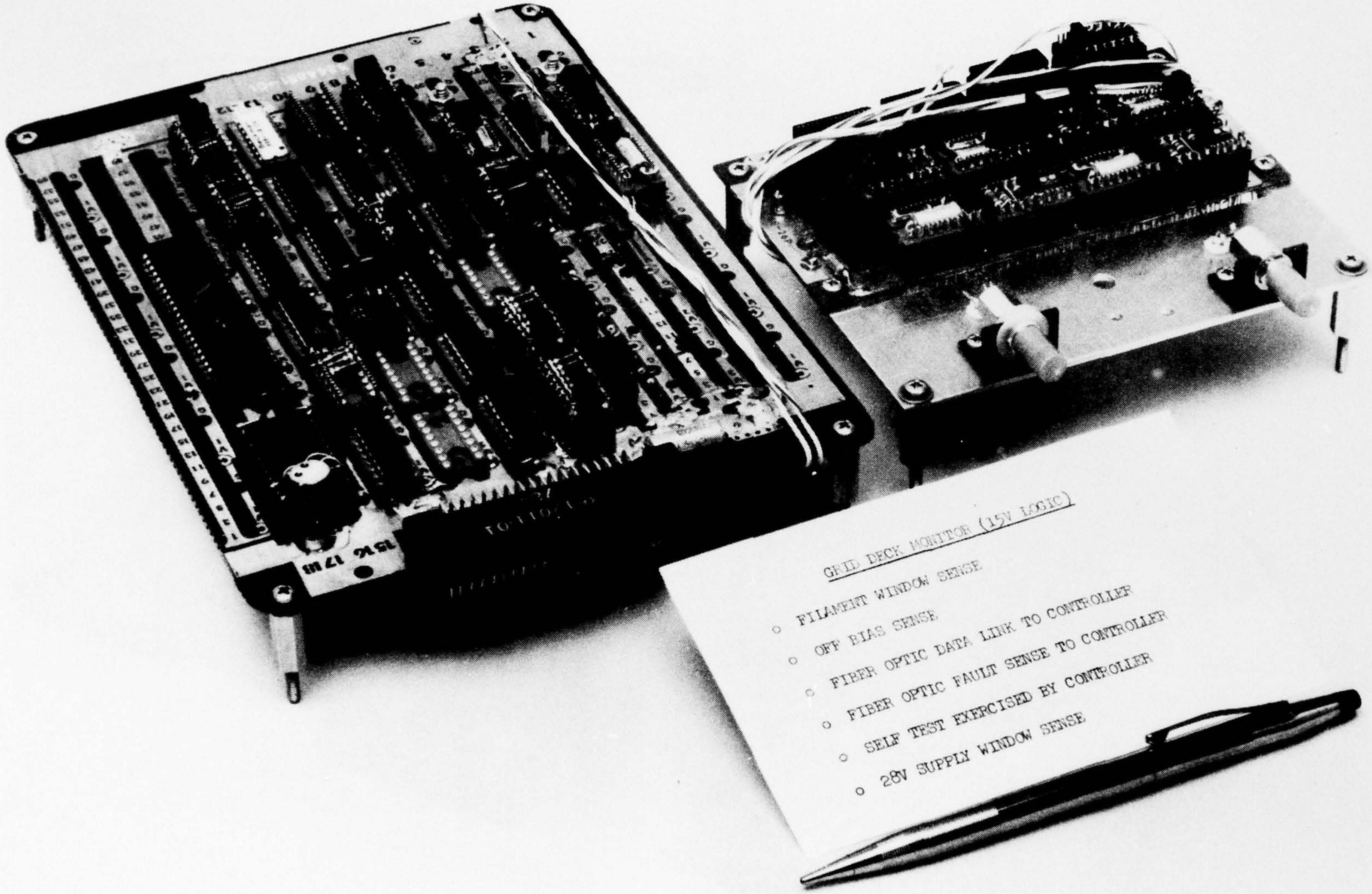

FIGURE 3 GRID DECK MONITOR CARDS

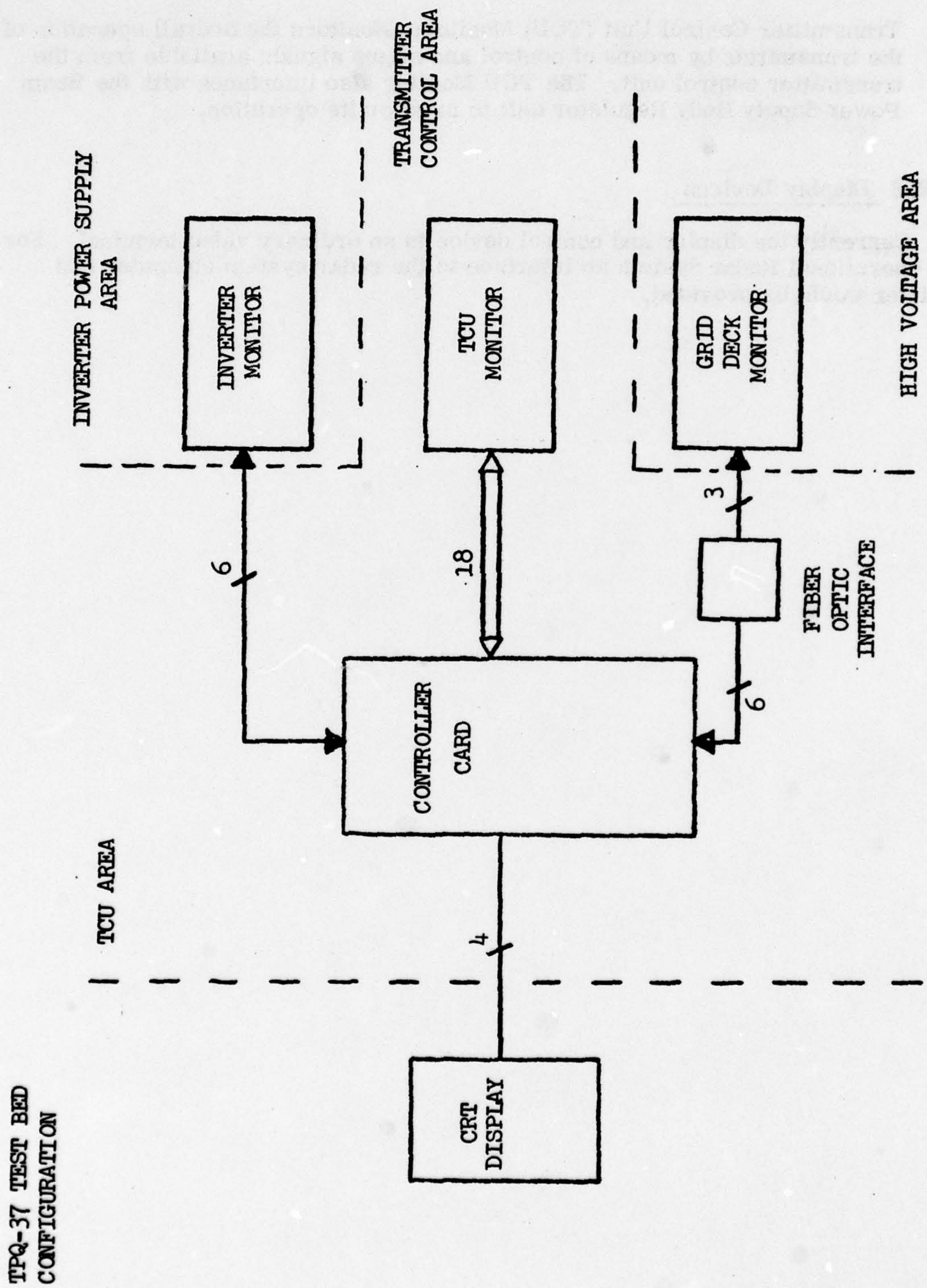

Figure 4. Fault Isolation Subsystem Block Diagram

2. Grid Deck Monitor: Monitors the operation of the Grid Deck Modulator and its associated power supplies. This circuit operates at the -42kV TWT cathode potential and interfaces with the Controller Card through a fiber optic link.

3. Transmitter Control Unit (TCU) Monitor: Monitors the overall operation of the transmitter by means of control and status signals available from the transmitter control unit. The TCU Monitor also interfaces with the Beam Power Supply Body Regulator unit to monitor its operation.

2.2.3 Display Devices

Currently the display and control device is an ordinary video terminal. For an operational Radar System an interface to the radar system computer and printer would be provided.

SECTION 3
FAULT ISOLATION TECHNIQUES

Section 3

FAULT ISOLATION TECHNIQUES

3.1 INTRODUCTION

The techniques to be used for transmitter fault isolation are similar to those used by maintenance personnel. That is a trained operator expects certain reactions to external stimulus in order to verify the operation of the transmitter. Any deviation from the expected reactions provides valuable information to an alert operator as to the possible cause of the problem. It is this technique which will be expanded upon in the fault isolation firmware logic.

The fault isolation subsystem will take advantage of, and in fact expand on the functional isolation provided by transmitter sequencing. That is, for any step in a sequence to be initiated, prior steps must have been successfully completed. This implies that the required circuits performed their function. Alternately if a step in the sequence failed to produce the expected results, only those circuits responsible for the functional step need be considered. It can be shown that reducing the functional complexity of each step in the sequence reduces the amount of circuitry to be considered by the fault isolation firmware.

The firmware in the controller card will use the status information provided by the transmitter monitor cards. The microprocessor will determine the current step or state and test for the expected result.

The functional isolation of the circuitry permits us to develop equations relating a fault to its possible causes. When a fault is detected these equations are used to further isolate the fault to a LRU.

3.2 DETAILED CIRCUIT DESCRIPTION

3.2.1 Controller Card

The Controller Card block diagram as shown in Figure 5, is based on an 8080A microprocessor and it's support circuits and provides:

- 16K bytes of programmable read only memory
- 8K bytes of read/write memory
- 7 levels of priority interrupt
- Serial interface channels to: Test Console
  Grid Deck Monitor
  Inverter Monitor
- Parallel 15 volt interface to TCU monitor

These features enable the microprocessor to detect faults and evaluate a series of fault equations which will isolate to the malfunctioning LRU and send a maintenance oriented report to the test console.

3.2.2 Monitor Cards

The Monitor Cards provide the interface from the transmitter to the Controller Card. The inputs to these monitor cards are many and varied and include:

- 28 and 15 volts bi-stable signals
- digital latched fault indicators to determine the first occured fault
- analog inputs to level comparators which convert analog signals to bi-stable go/no-go signals
- Analog peak detection circuits used to validate pulsed analog signals
- Analog levels which feed an analog to digital converter directly

In addition to being the recipient of input information the monitor cards provide latched bi-stable and analog voltage outputs. The bi-stable outputs serve two main functions. First they provide the stimulus for the self test logic. Second, they provide control signals used by the fault isolation logic to slow the transmitter turn on sequence. This allows sufficient time for collection of time critical status information.

The two analog outputs are control outputs used in the cathode current and RF drive saturation control loops.

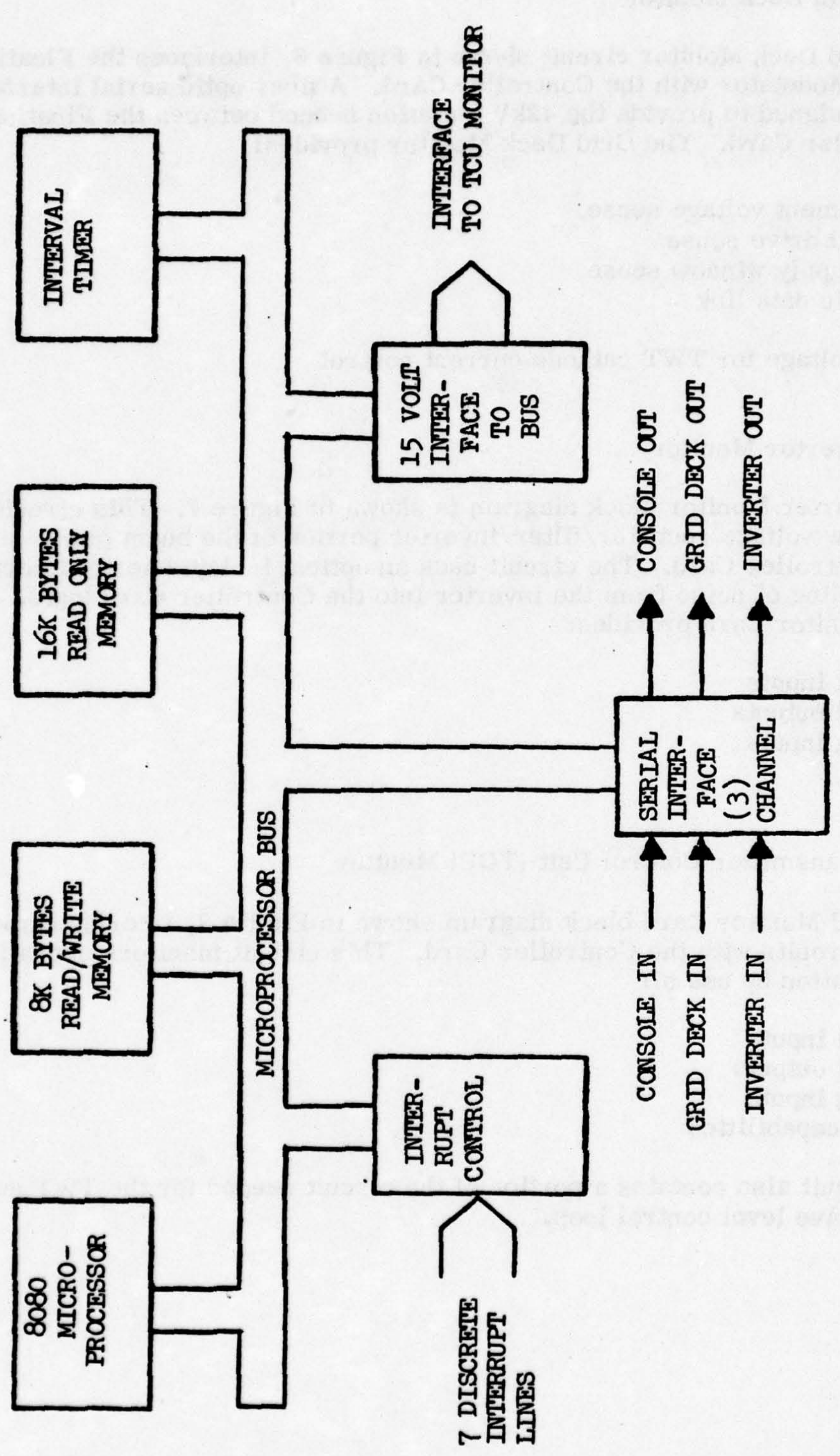

Figure 5. Microprocessor Based Controller Card

3.2.2.1 Grid Deck Monitor

The Grid Deck Monitor circuit shown in Figure 6, interfaces the Floating Deck Grid Modulator with the Controller Card. A fiber optic serial interface has been designed to provide the 42kV isolation needed between the Floating Deck and Controller Card. The Grid Deck Monitor provides:

- TWT filament voltage sense
- TWT grid drive sense
- 28 volt supply window sense
- fiber optic data link
- Self test
- Analog voltage for TWT cathode current control

3.2.2.2 Inverter Monitor

The Inverter Monitor block diagram is shown in Figure 7. This circuit interfaces the low voltage rectifier/filter/inverter portion of the beam power supply with the Controller Card. The circuit uses an optical isolated serial interface to reduce coupling of noise from the inverter into the Controller Card logic. The inverter Monitor Card provides:

- 24 digital inputs
- 16 digital outputs
- 16 analog inputs
- Self test

3.2.2.3 Transmitter Control Unit (TCU) Monitor

The TCU Monitor Card block diagram shown in Figure 8, interfaces the TCU 15V logic circuits with the Controller Card. This circuit monitors overall transmitter operation by use of:

- 64 digital inputs
- 16 digital outputs
- 16 analog inputs
- Self test capabilities

The circuit also contains a portion of the circuit needed for the TWT automatic RF drive level control loop.

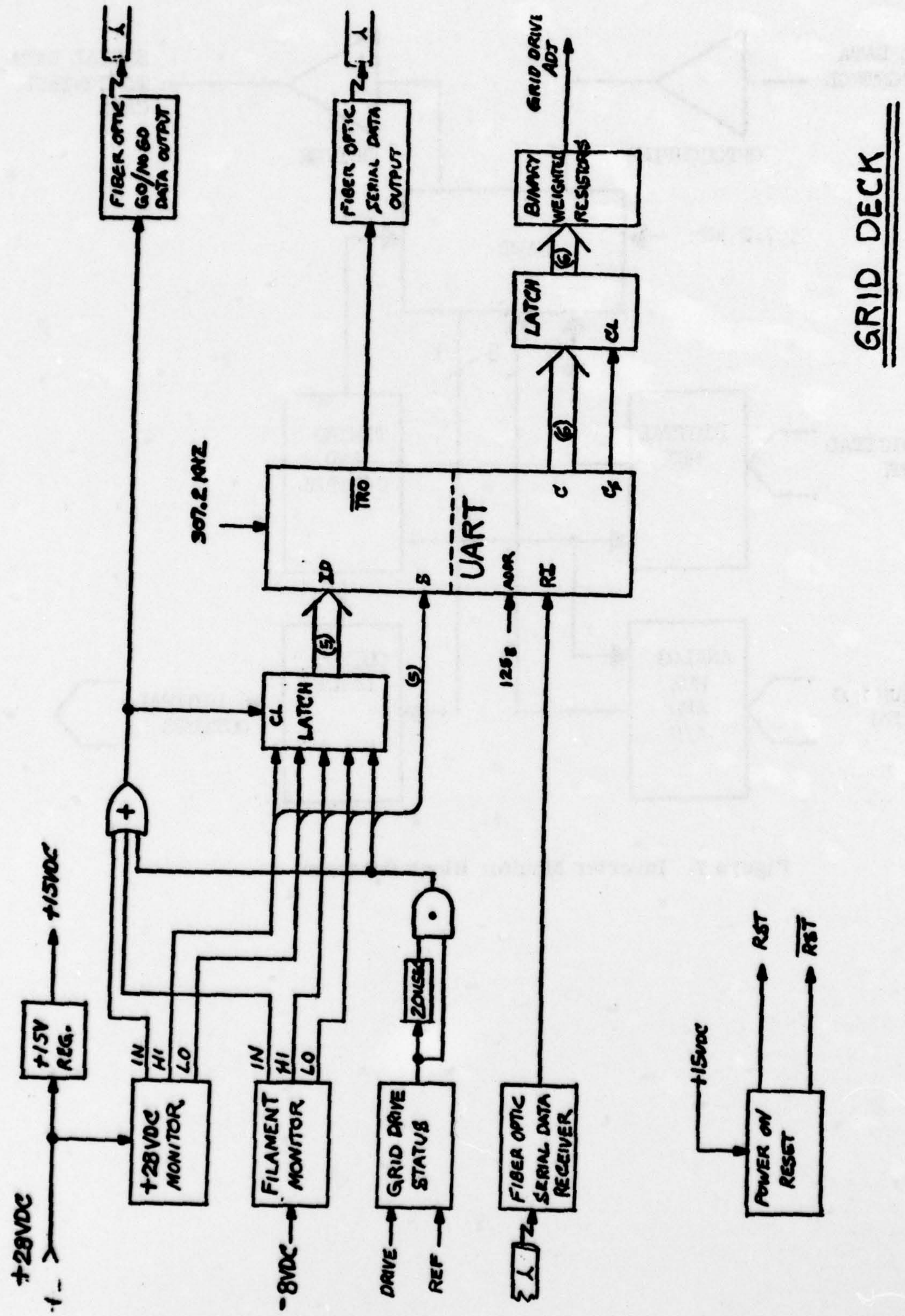

Figure 6. Grid Deck Monitor

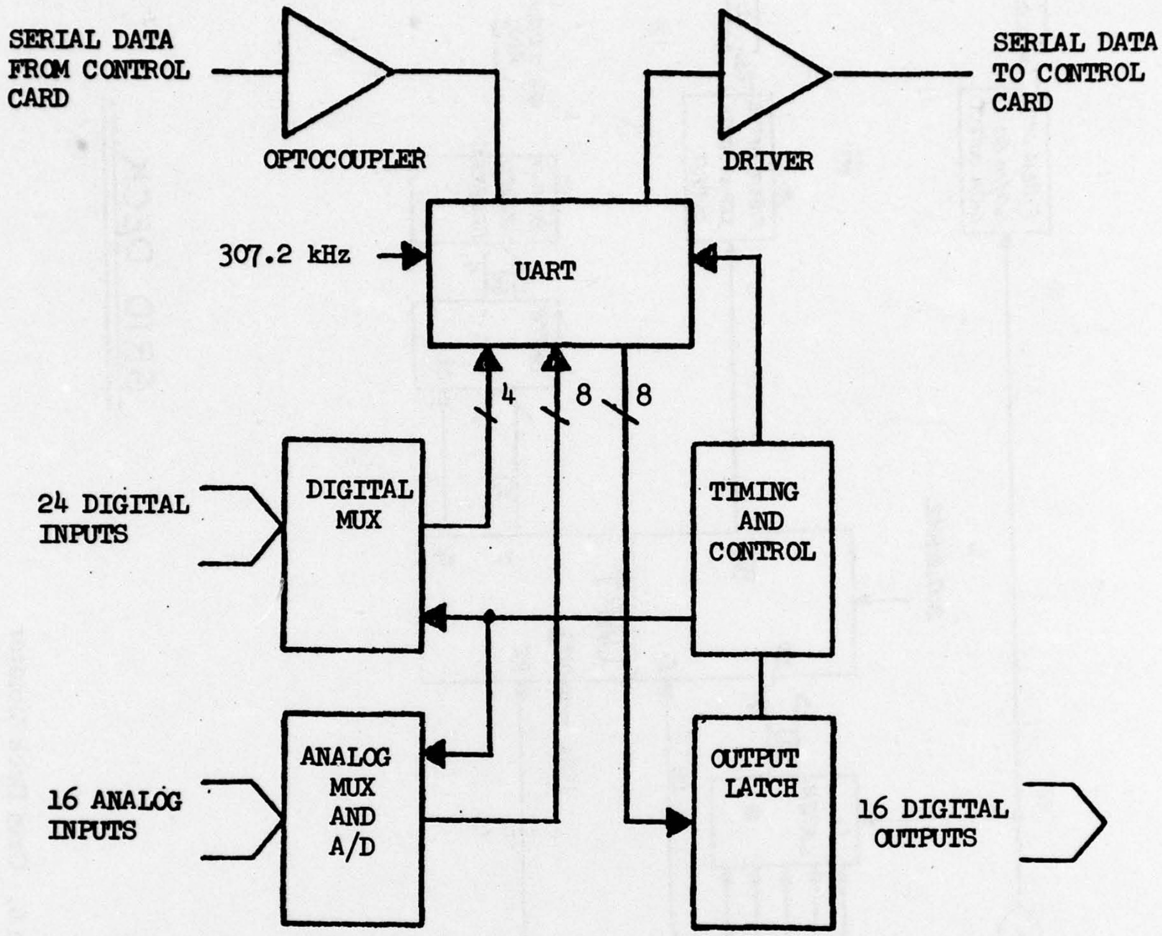

Figure 7. Inverter Monitor Block Diagram

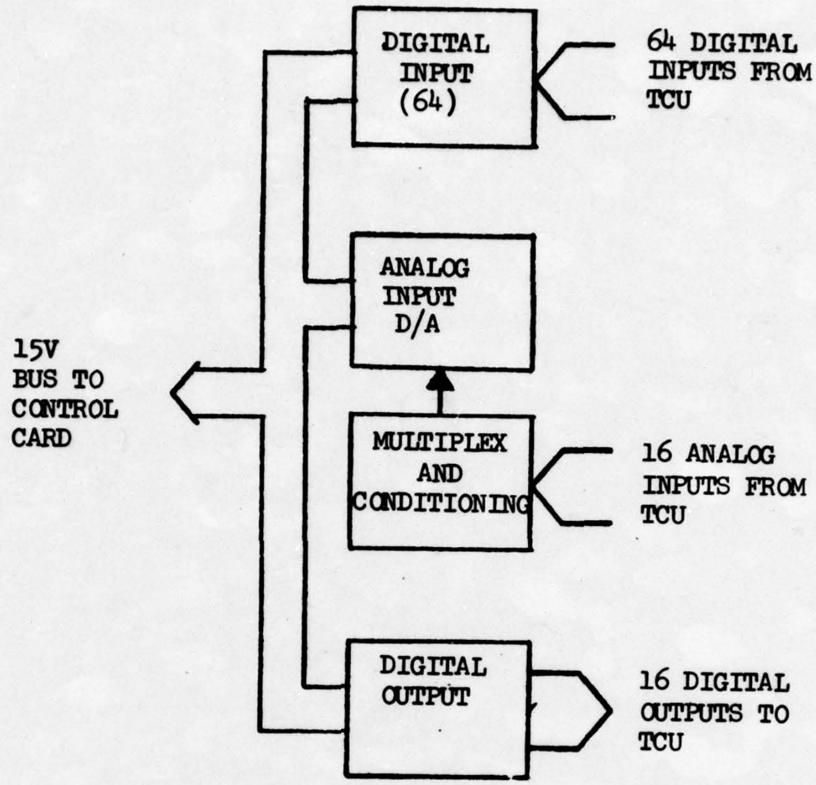

Figure 8. Transmitter Control Unit Monitor

SECTION 4
AUTOMATIC CATHODE CURRENT CONTROL LOOP

AUTOMATIC CATHODE CURRENT CONTROL LOOP

The automatic cathode current control loop (CCCL) maintains the TWT peak cathode current at the nameplate value, despite such effects as decreased emission with tube aging and temperature induced distortion of the heater-cathode-grid structure. With the CCCL, the maintenance effort is also reduced and the possibility of inadvertent, but harmful mis-adjustment of the current level is eliminated.

The present design shown in Figure 9, routes the signal from the existing body and collector current sensors to the Controller Card. The sum of these currents equals the cathode current, which is compared with the nameplate value. If an adjustment is required the microprocessor computes the change and transmits the new value to the analog control circuit on the Floating Deck Grid Monitor. There the Grid Deck Monitor provides the compensated control voltage to the pulse top regulator to correct the cathode current.

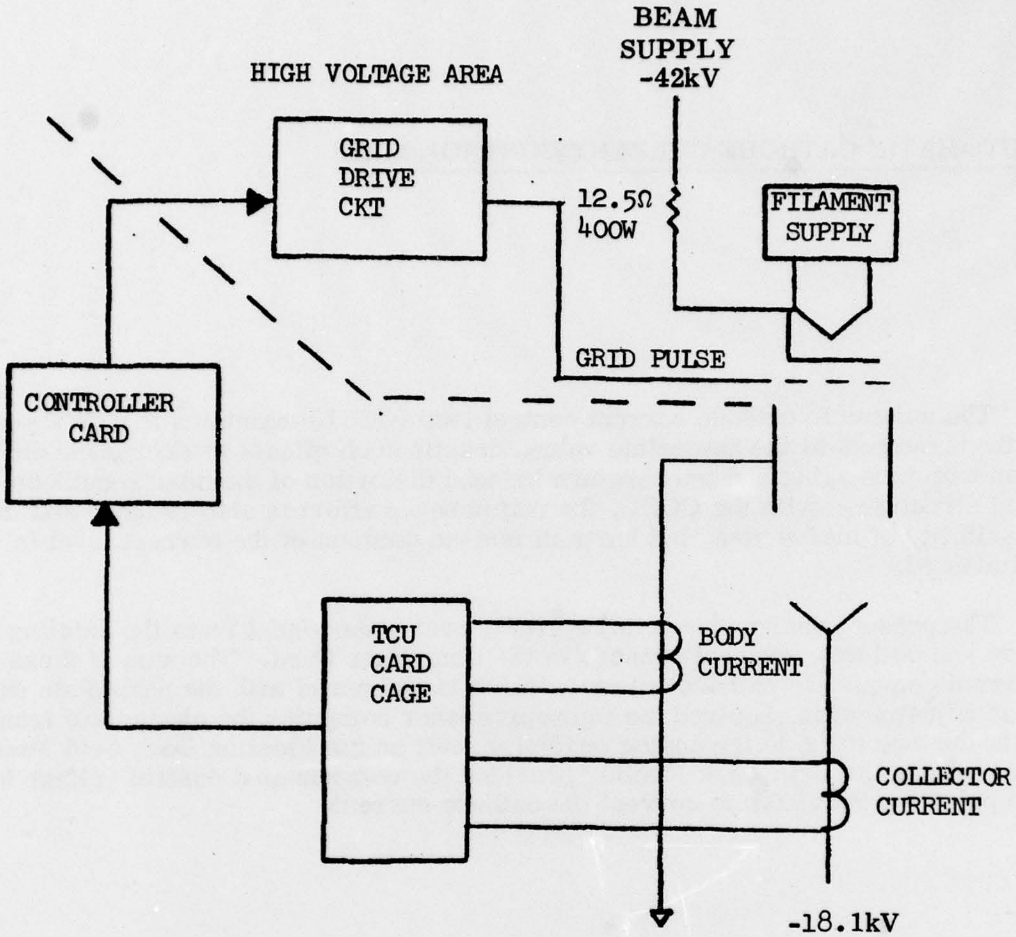

Figure 9. Cathode Current Control Loop (CCCL).

SECTION 5
AUTOMATIC RF DRIVE LEVEL CONTROL LOOP

AUTOMATIC RF DRIVE LEVEL CONTROL LOOP

The RF drive level necessary to saturate a TWT is a function of the operating frequency. In addition, the optimum RF drive level will also change with tube age and circuit parameters such as cathode voltage. These variations can easily result in the TWT being either over or under driven. Under driving the TWT causes no harmful effects, but does degrade RF output power. Overdriving the TWT will, on the other hand, not only degrade RF output power, but will also increase the tube body current. Thus, automatic RF drive level control is desirable to provide peak RF performance as well as protect the tube from the harmful effects of overdrive.

Figure 10 shows a block diagram of a proposed RF drive level control loop. This circuit samples the RF output of the TWT for a given drive input. By varying the attenuation of the PIN diode attenuator, in a controlled manner, the microprocessor can determine the optimum drive level required to just achieve saturation. This drive level thus determined is valid only at that specific frequency.

The above mechanization is under study and its effect on transmitter stability and radar system doppler processing performance is being evaluated.

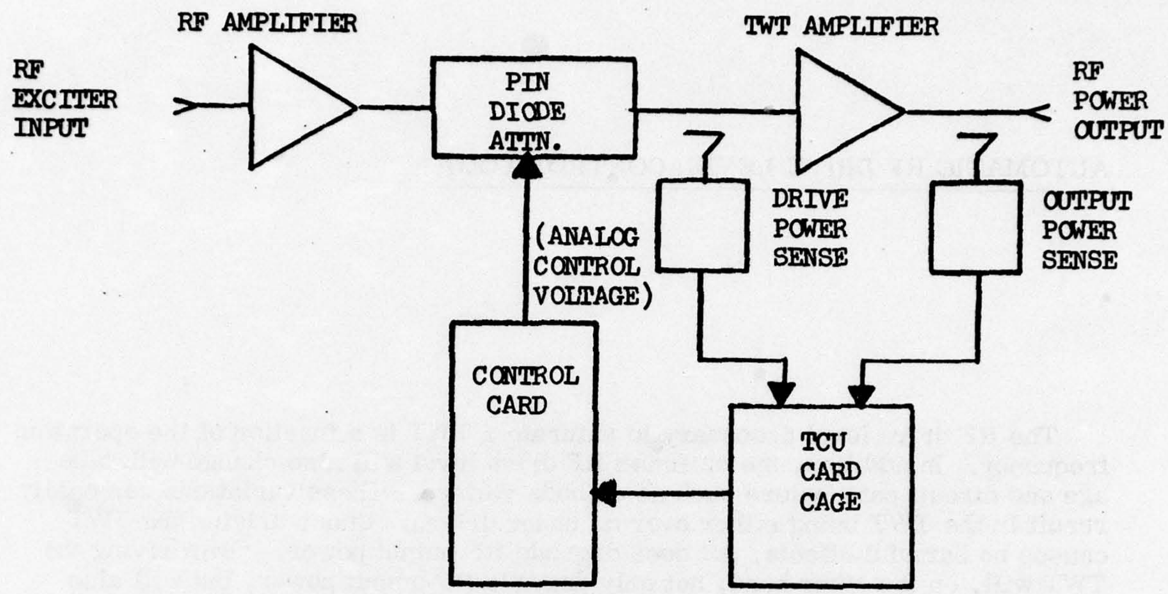

Figure 10. Proposed RF Drive Saturation Loop

SECTION 6
CONCLUSION

Section 6

CONCLUSION

During this first reporting period the design on the fault isolation subsystem has been largely completed, and a substantial portion of the hardware has been fabricated and assembled. Initial tests of the circuitry are under way, and no obstacle to successful completion of the program is foreseen.

Ground work has also been laid for integrating the new TWT and Floating Deck Grid Modulator into the AN/TPQ-37 transmitter test bed.

Discussions with ERADCOM and Firefinder are continuing in an effort to identify the transmitter to be used for the evaluations required by this program. Subsequently, a schedule will be worked out.

SECTION 7
SUBSEQUENT PROGRAM DIRECTION

Section 7

SUBSEQUENT PROGRAM DIRECTION

Bench testing of the fault isolation hardware will continue concurrent with development of the firmware. The cathode current and RF drive level control loops will be included in the fault isolation hardware. Subsequent to this, the subsystem will be evaluated in the test bed transmitter.

Evaluation of the new TWTs, the Solid State Grid Modulator, and the commutating choke design work will be paced to coincide with availability of the (GFP) test bed transmitter. A schedule for these efforts and the availability of the production transmitter, to be used as the test bed, should be available shortly.

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